WHAT IS CLAIMED IS:

1. An image sensor, comprising:

multiple pixels each including a respective photodiode region;

pixel circuits each operable to control integration and readout steps for a respective pixel; and

a bias circuit operable to apply voltages across the pixels to induce carrier injection into the photodiode regions to reduce image lag.

2. The image sensor of claim 1, wherein the bias circuit is operable to induce forward bias flow of injected carriers through the pixel photodiode regions.

3. The image sensor of claim 2, wherein the bias circuit is operable to periodically induce forward bias flow of injected carriers through photodiode regions.

4. The image sensor of claim 3, wherein the pixel circuits and the bias circuit are cooperatively configured so that forward bias flow of injected carriers occurs during a reset step for each pixel.

5. The image sensor of claim 2, wherein pixels are arranged in an array of multiple rows and the bias circuit is operable to simultaneously induce forward bias flow of injected carriers through the photodiode regions of all pixels in a given row of the array.

6. The image sensor of claim 5, wherein the bias circuit is operable to simultaneously induce forward bias flow of injected carriers through the photodiode regions one row at a time.

7. The image sensor of claim 6, wherein the bias circuit is operable to simultaneously induce forward bias flow of injected carriers through photodiode regions of a given row before the pixel circuits in the given row initiate an integration step for the given row.

8. The image sensor of claim 5, wherein the bias circuit is operable to simultaneously induce forward bias flow of injected carriers through photodiode regions of all rows in the array.

9. The image sensor of claim 1, wherein the bias circuit is operable to induce carrier injection between photodiode regions of pixels.

10. The image sensor of claim 10, wherein the bias circuit is operable to induce carrier injection between photodiode regions of adjacent pixels.

11. The image sensor of claim 10, wherein the bias circuit is operable to apply different voltages levels to nodes of adjacent pixels.

12. The image sensor of claim 11, wherein the bias circuit is operable to apply different high-to-low voltage ranges across adjacent pixels.

13. The image of sensor of claim 11, wherein pixels are arranged in an array of multiple rows and the bias circuit is operable to apply different voltage levels to nodes of adjacent pixels in adjacent rows.

14. The image sensor of claim 11, wherein pixels are arranged in an array of rows and columns and the bias circuit is operable to apply different voltage levels to nodes adjacent pixels in adjacent rows and to apply different voltage levels to nodes of adjacent pixels in adjacent columns.

15. The image sensor of claim 10, wherein the different voltage levels applied to nodes of adjacent pixels are switched periodically.

16. The image sensor of claim 10, wherein the bias circuit includes two bias lines for applying different respective voltage levels to the pixels.

17. The image sensor of claim 10, wherein the bias circuit includes a bias line and a set of resistive elements respectively coupled in parallel between the bias line and alternate pixels.

18. A method of operating an image sensor comprising multiple pixels each including a respective photodiode region, the method comprising:

resetting photodiode regions;

integrating charge in photodiode regions;

sampling pixel nodes; and

inducing carrier injection into photodiode regions to reduce image lag.

19. The method of claim 18, wherein inducing carrier injection comprises inducing forward bias flow of carriers through the pixel photodiode regions.

20. The method of claim 18, wherein inducing carrier injection comprises inducing carrier injection between photodiode regions of adjacent pixels.